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DynaOpt: A Heterogeneous Logic Optimization Framework

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Background & Motivation

EDA Logic Synthesis: transforms HDL to gate-level netlists by applying a sequence of logic transformations

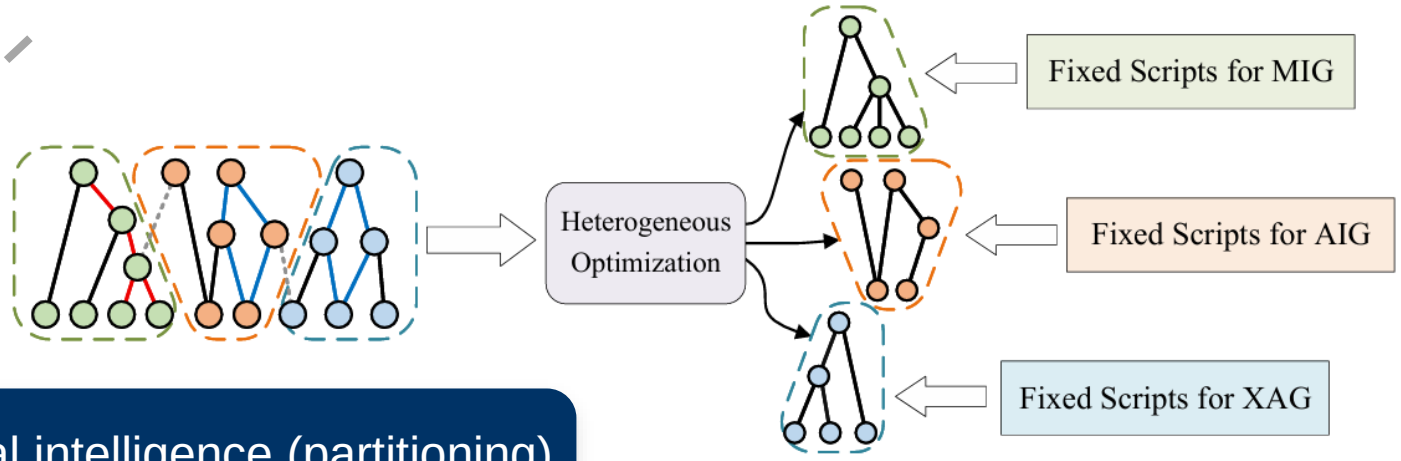
Dynamic Sequence Generation

☑ Custom optimization flows.
✗ Ignores internal structural diversity (Blind to the "where").

V.S.

Heterogeneous Logic Optimization

☑ Best data structure per region (AIG, MIG, XAG).
✗ Relies on fixed, pre-defined scripts (Limited in the "how").



The Missing Link: How to unify the spatial intelligence (partitioning) with the procedural intelligence (dynamic sequences)?

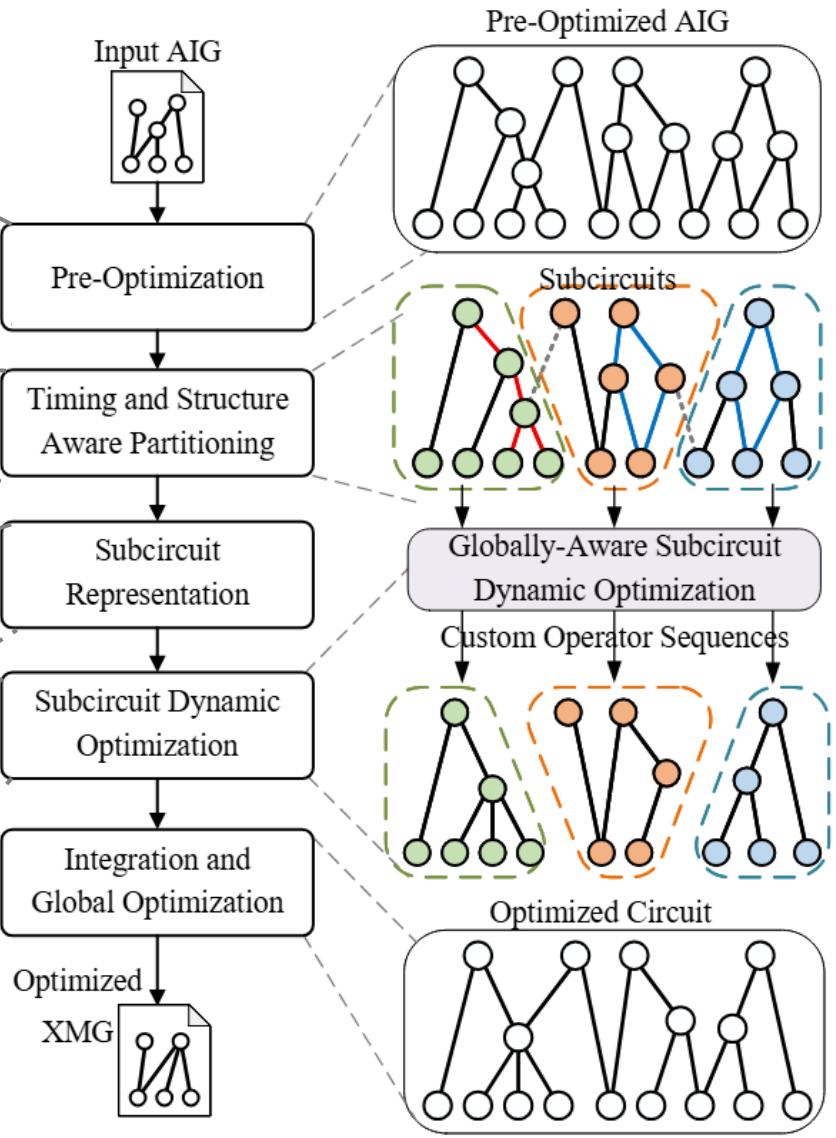
DynaOpt Framework: Overview

Global Pre-Opt: Transformer clears superficial redundancies.

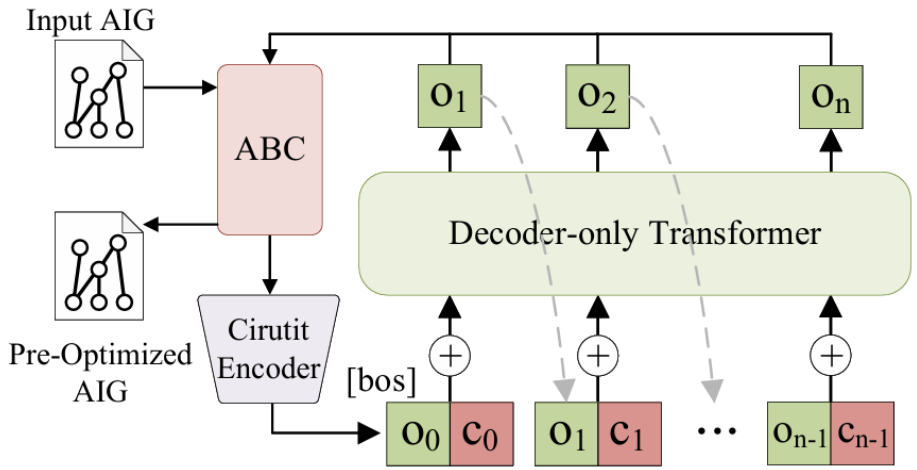
Smart Partitioning: Timing & structure-aware cuts.

DAG Selection: GNN predicts optimal AIG/MIG/XMG.

Dynamic Sequences: GA generates bespoke flows guided by global fitness.

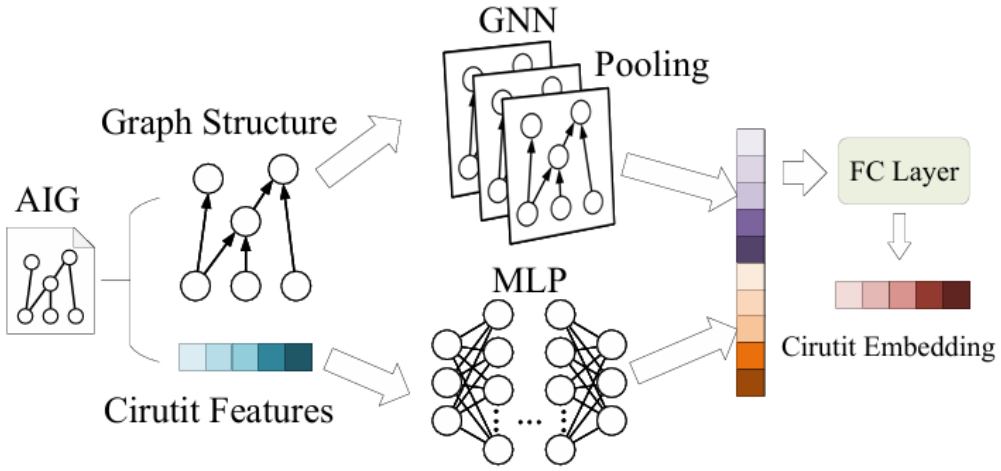


Global Pre-Optimization



The Problem

- Raw networks contain superficial redundancies.
- Leads to suboptimal partitioning.



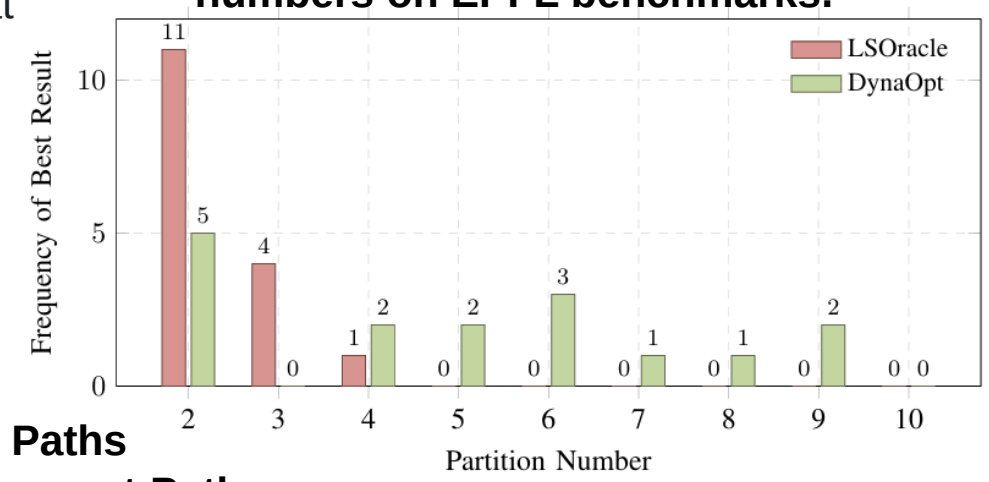
The Solution

- A learning-based, decoder-only Transformer.
- Autoregressively predicts tailored optimization sequences.
- Uses a Dual-input Encoder
  (GNN for topology + MLP for features).

Partitioning

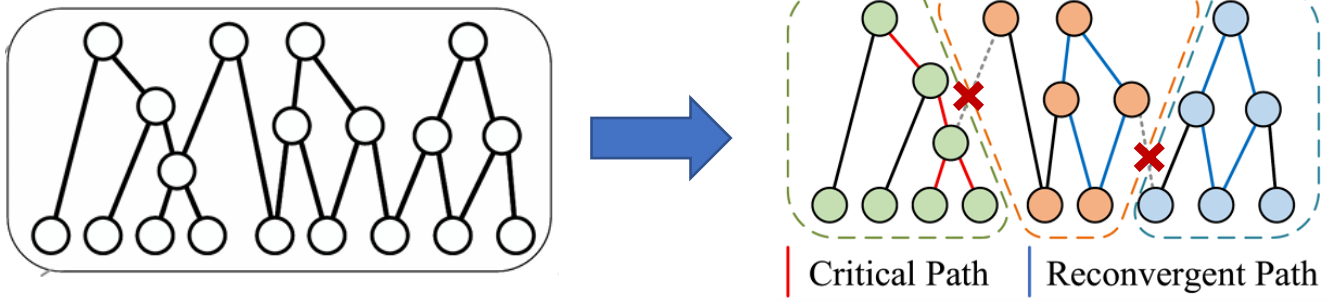
The Problem:
Standard tools fail at high granularity.

Fig. 3 Best result distribution over partition numbers on EPFL benchmarks.

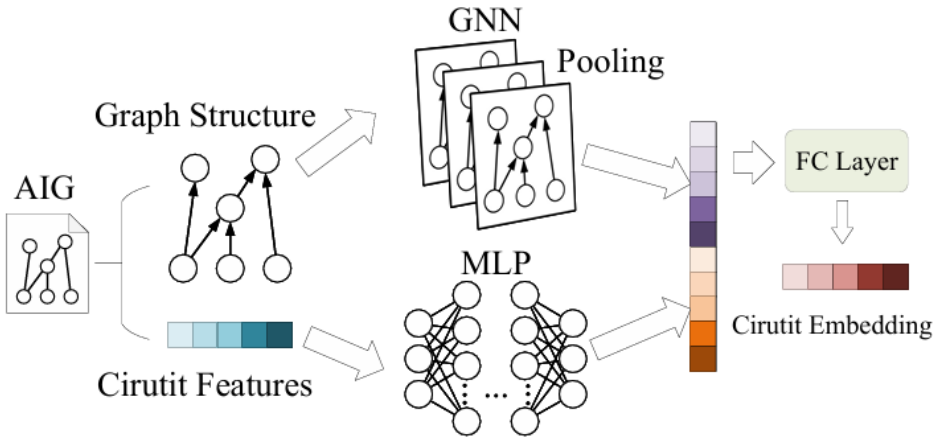


The Solution

- Protects **Critical Paths**
- Protects **Reconvergent Paths**
- Protects **High-fanout nets**



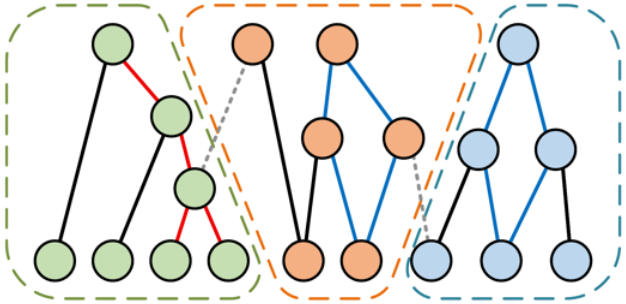
Subcircuit Representation

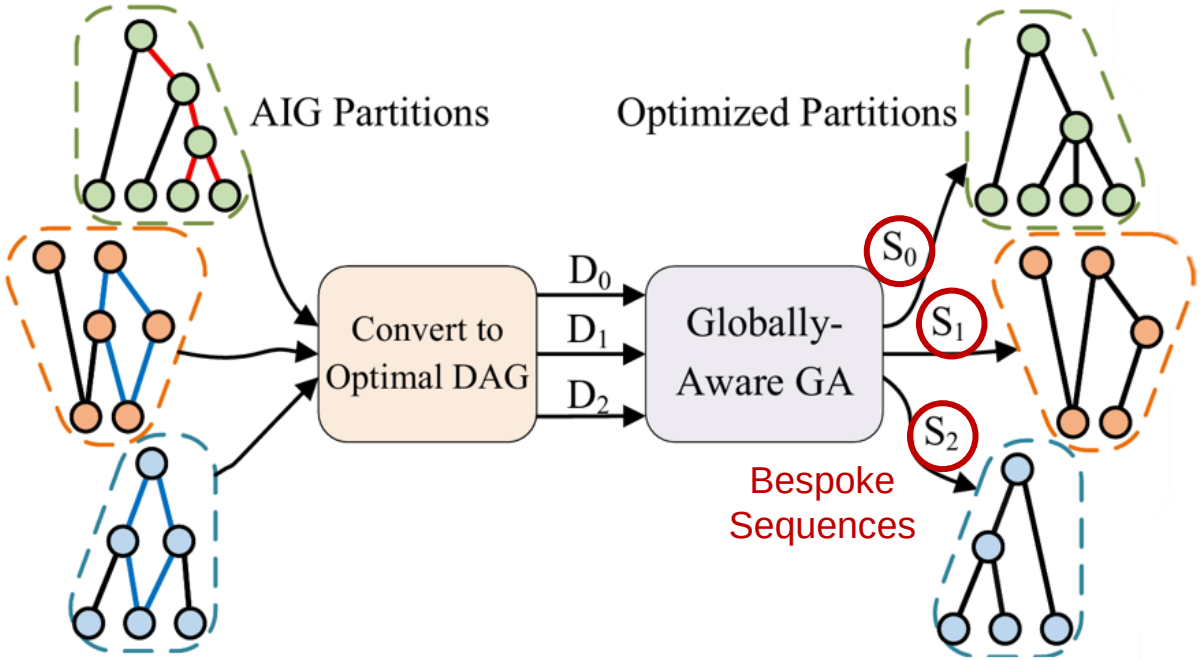


Goal: Maximize potential of each partition.
Method: Dual-input encoder (GNN + MLP).
Output: Predicts optimal AIG, MIG, XAG, or XMG.

Globally-Aware Subcircuit Dynamic Optimization

The Workflow





Fitness Function

The Trap: Local Gains ≠ Global Optimality
Fitness = Original Global NDP − Estimated New Global NDP

$$N'_g = N_g - \Delta N_l.$$

$$D'_g = \begin{cases} D_g - \Delta D_l, & \text{if on crit. path,} \\ \max(D_g, D_{l,\text{new}}) - \lambda \cdot \Delta D_l, & \text{otherwise.} \end{cases}$$

$$\text{Fitness} = (N_g \cdot D_g) - (N'_g \cdot D'_g).$$

Experimental Results

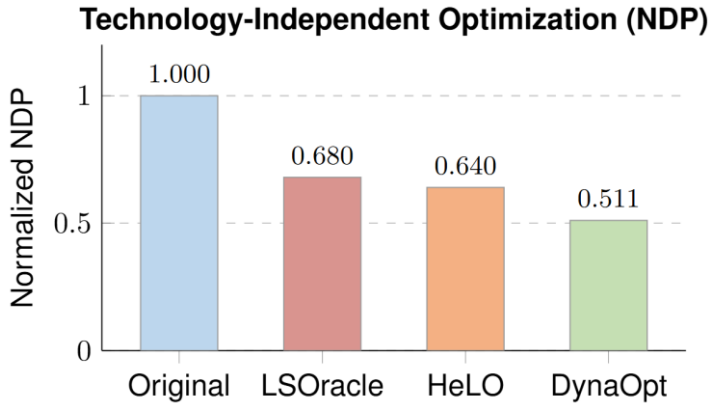
TABLE I Technology-independent logic optimization result. NDP denotes the product of node count and depth.

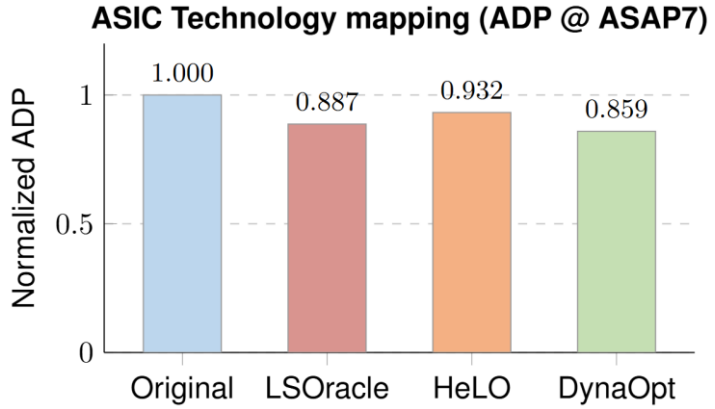
Circuit	Original			LSOracle [14]			HeLO [10] *			DynaOpt (Ours)		
	node	level	NDP	node	level	NDP	node	level	NDP	node	level	NDP
pico-rv	14551	31	451081	15124	18	272232	19268	18	346824	12780	15	**191700**
chip_bridge	58596	31	1816476	59180	19	1124420	58317	19	1108023	57532	17	**978044**
s38417	8594	28	240632	9198	19	174762	9522	16	152352	8271	16	**132336**
fpu	65750	33	2169750	60955	20	1219100	68099	20	1361980	60466	18	**1088388**
aes_core	13232	44	582208	14318	29	415222	21867	18	393606	9968	26	**259168**
des_perf	82373	20	1647460	79784	16	1276544	70176	15	**1052640**	76482	14	1070748
ethernet	67164	33	2216412	64909	22	1427998	71896	20	1437920	61065	20	**1221300**
dyn_node	3986	27	107622	4113	19	78147	4034	18	72612	3798	14	**53172**
vga_lcd	105334	22	2317348	102031	19	1938589	101534	17	1726078	103788	15	**1556820**
fpga_bridge	318081	41	13041321	312498	31	9687438	324356	24	7784544	322419	20	**6448380**
i2c	1342	20	26840	1404	10	14040	1385	8	11080	1168	8	**9344**
mem_ctrl	46836	114	5339304	52819	69	3644511	56592	61	3452112	46258	54	**2497932**
normalize	1.000	1.000	1.000	1.018	0.669	0.680	1.106	0.591	0.640	0.929	0.551	**0.511**

TABLE II ASIC technology mapping result using ASAP7 PDK. ADP denotes the product of delay (ps) and area (um^2).

Circuit	Original			LSOracle [14]			HeLO [10] *			DynaOpt (Ours)		
	area	delay	ADP	area	delay	ADP	area	delay	ADP	area	delay	ADP
pico-rv	700.7	325.2	227850.4	618.6	269.5	166728.6	831.6	290.0	241153.0	564.0	283.8	**160051.9**
chip_bridge	2657.2	308.9	820871.5	2613.4	293.6	**767247.8**	3028.2	263.9	799010.0	2512.1	317.1	796448.6
s38417	418.7	314.7	131790.0	428.9	296.7	127280.7	416.2	266.7	**111016.0**	420.6	296.2	124578.0
fpu	2751.4	396.5	1090926.1	2765.4	341.0	**943098.4**	3127.9	324.8	1016209.0	2873.2	336.0	965449.3
aes_core	573.1	511.8	293308.1	615.6	441.7	271895.5	1061.0	251.0	266276.0	562.0	451.9	**253954.4**
des_perf	4459.3	264.8	1180943.2	4492.9	239.1	1074117.6	3457.8	232.8	**804807.0**	4210.7	249.1	1049009.2
ethernet	3131.6	345.1	1080736.1	2872.1	342.4	983464.5	3407.0	289.4	985948.0	2739.1	314.5	**861461.8**
dyn_node	190.1	299.5	56932.0	196.5	241.0	**47353.2**	205.5	231.7	47610.0	199.4	240.9	48026.2
vga_lcd	4766.1	387.1	1844898.0	4676.2	340.2	1591043.9	5627.5	259.5	1460459.2	4292.4	338.8	**1454100.2**
fpga_bridge	14044.7	515.1	7234430.1	14997.7	430.1	6451123.6	16385.7	340.9	**5585048.8**	14458.8	455.7	6588735.1
i2c	53.2	132.1	7024.8	60.3	107.0	6451.3	60.2	131.7	7931.6	57.4	107.4	**6164.6**
mem_ctrl	1826.5	997.9	1822553.1	1935.5	849.0	1643125.7	2395.2	1021.3	2446214.2	1841.7	826.8	**1522807.8**
normalize	1.000	1.000	1.000	1.014	0.877	0.887	1.170	0.812	0.932	0.972	0.886	**0.859**

HeLO* is non-open source, and results are quoted from original paper. The discrepancy primarily arises from Verilog-to-AIG conversion.





- **Best on 11/12 Benchmarks (NDP)**
- **24.9% Improvement over LSOracle Baseline**
- **Lowest ADP: 0.859 @ ASAP 7nm**

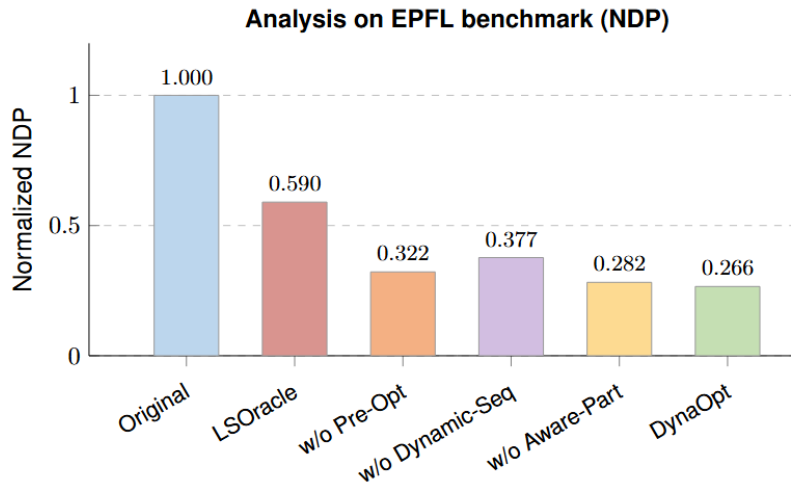
Experimental Results

TABLE III In-depth analysis and ablation study on the EPFL benchmark suite.

benchmark	Original			LSOracle [14]			w/o Pre-Opt			w/o Dynamic-Seq			w/o Aware-Part			DynaOpt (Ours)		
	node	level	NDP	node	level	NDP	node	level	NDP	node	level	NDP	node	level	NDP	node	level	NDP
adder	1020	255	260100	1697	21	35637	1459	19	27721	1896	19	36024	1203	18	**21654**	1633	14	22862
cavlc	693	16	11088	707	15	10605	631	11	6941	663	11	7293	608	11	6688	627	10	**6270**
ctrl	174	10	1740	128	7	896	108	5	540	98	5	490	94	5	**470**	95	5	475
div	57247	4372	250283884	121464	841	102151224	74606	1171	87363626	60763	814	49461082	84798	684	58001832	39222	668	**26200296**
i2c	1342	20	26840	1404	10	14040	1356	8	10848	1256	8	10048	1196	7	**8372**	1188	8	9504
int2float	260	16	4160	251	13	3263	236	8	1888	217	10	2170	208	9	1872	220	8	**1760**
log2	32060	444	14234640	38853	281	10917693	32903	160	**5264480**	36692	224	8219008	33697	171	5762187	32635	162	5286870
max	2865	287	822255	4361	70	305270	3525	51	179775	3066	52	159432	4317	27	116559	3770	28	**105560**
mem_ctrl	46836	114	5339304	52819	69	3644511	54642	48	2622816	48246	53	2557038	54891	46	2524986	43060	53	**2282180**
multiplier	27062	274	7414988	37351	139	5191789	29647	88	**2608936**	33240	118	3922320	46445	57	2647365	32014	83	2657162
priority	978	250	244500	1054	130	137020	568	96	54528	624	61	38064	518	45	23310	539	43	**23177**
router	257	54	13878	415	17	7055	205	11	**2255**	242	11	2662	225	11	2475	234	11	2574
sin	5416	225	1218600	6483	141	914103	5865	97	568905	5653	122	689666	6736	91	612976	5399	91	**491309**
sqrt	24618	5058	124517844	17863	5061	90404643	27310	764	20864840	17266	4034	69651044	27482	681	**18715242**	24043	930	22359990
square	18484	250	4621000	22161	50	1108050	14627	38	555826	19020	43	817860	11787	27	**318249**	12986	29	376594
voter	13758	70	963060	10310	76	783560	7584	42	318528	8090	51	412590	4666	39	**181974**	4949	41	202909
normalize	1.000	1.000	1.000	1.210	0.560	0.590	0.976	0.352	0.322	0.977	0.421	0.377	0.997	0.313	0.282	0.900	0.321	**0.266**

TABLE IV Runtime comparison in seconds (s).

Circuit	LSOracle [14]	DynaOpt (Ours)
adder	6	32
cavlc	7	166
ctrl	4	67
div	634	2094
i2c	6	54
int2float	4	13
log2	314	611
max	12	83
mem_ctrl	340	519
multiplier	189	993
priority	6	76
router	4	24
sin	37	155
sqrt	101	534
square	90	569
voter	54	166
normalize	0.228	1.000



Ablation Study (Normalized NDP)

Full DynaOpt	**0.266**
w/o Aware-Part	0.282
w/o Pre-Opt	0.322
w/o Dynamic-Seq	0.377

- **Lowest Average NDP: 0.266 (Full DynaOpt)**
- **Dynamic-Seq is the Key Driver (Biggest drop to 0.377)**
- **A Direct Trade-off: ~4.4x runtime for significantly better QoR**

Conclusion

1. A New Paradigm: Replaces static scripts with fully adaptive, bespoke optimization sequences.

2. Holistic Framework: Unifies smart partitioning, GNN DAG selection, and globally-aware GA.

3. SOTA Performance: Delivers superior logic (NDP) and physical (ADP) Quality-of-Results.

THANK YOU !