DynaOpt: A Heterogeneous Logic Optimization Framework with Dynamic Sequence Generation

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Introduction

Problem: Fixed optimization sequences yield suboptimal results for diverse circuits. Two advanced research frontiers attempt to solve this, but each has a critical blind spot:

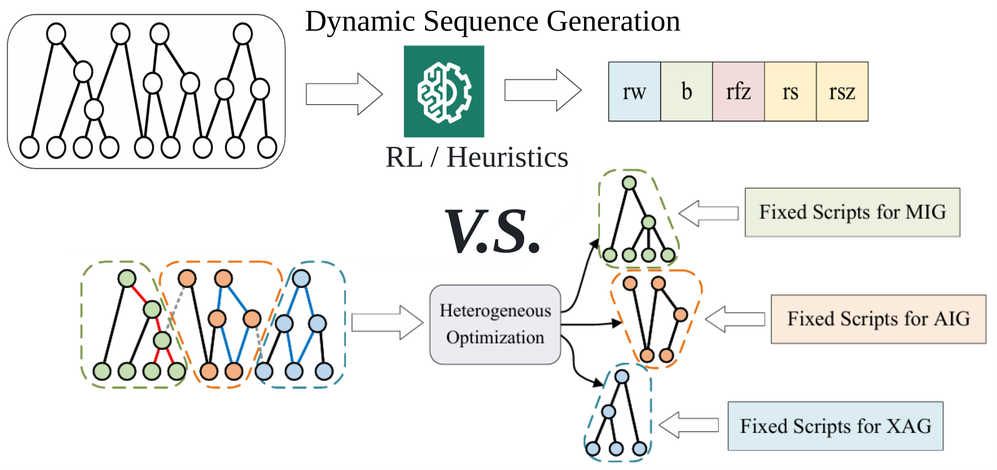
Frontier 1: Dynamic Sequence Generation

Generates superior, circuit-specific optimization flows. Treats circuits monolithically, ignoring internal structural diversity (masters the "how", blind to the "where").

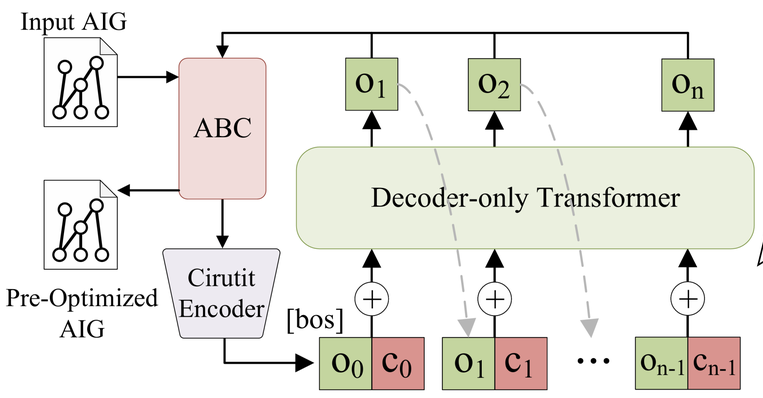
Frontier 2: Heterogeneous Logic Optimization

Partitions circuits to apply the best-fit data structures (AIG, MIG, XAG) to different regions. Relies on static, pre-defined optimization scripts for each partition (masters the "where", limited in the "how").

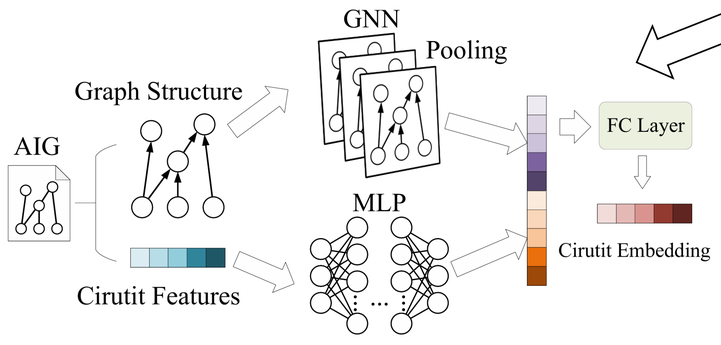
Our Solution: DynaOpt Bridges this critical gap by unifying the spatial intelligence of heterogeneous partitioning with the procedural intelligence of dynamic sequence generation, crafting bespoke strategies for every sub-circuit.



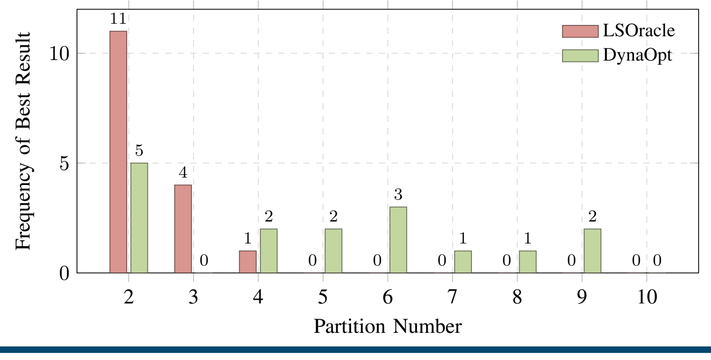
Methodology

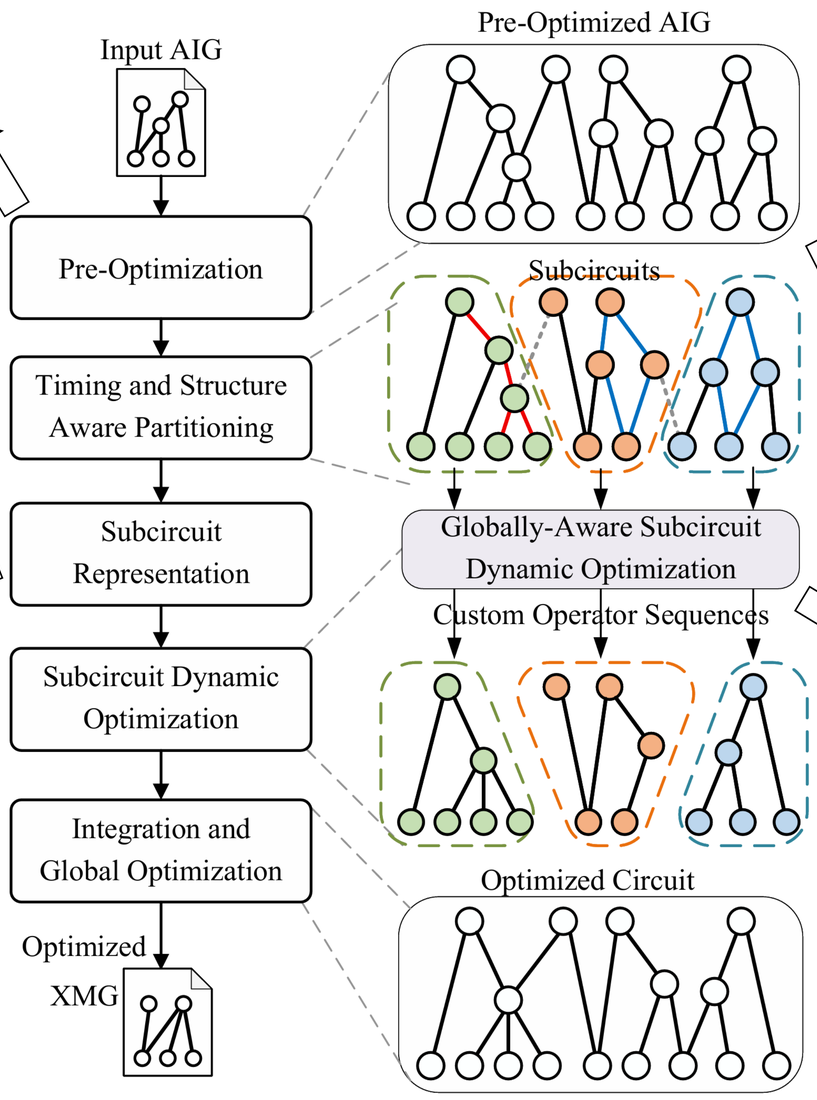


Global Pre-Optimization. To eliminate superficial redundancies, a decoder-only Transformer autoregressively generates and applies tailored optimization sequences. This refines the netlist and enhances downstream partitioning quality.

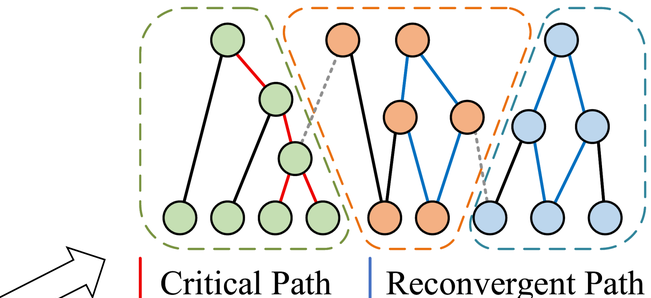


Sub-Circuit Representation. A GNN classifier automates optimal DAG selection. A dual-input encoder (3-layer GAT for topology, MLP for scalar features) predicts the best representation to maximize each partition's potential.

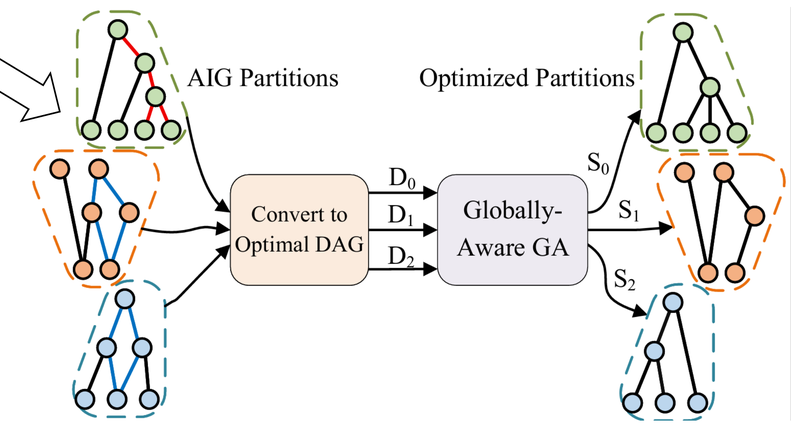




Overall Workflow. DynaOpt refines networks via model-based pre-optimization and timing/structure-aware partitioning. A GNN selects the optimal DAG per partition. A GA then generates custom sequences using a global fitness function, before unifying all partitions into XMG.



Timing and Structure-Aware Partitioning. A customized hypergraph partitioner minimizes connectivity (fewer PIs/POs). To prevent severing critical structures, we dynamically assign higher weights to preserve: (1) critical paths (timing), (2) reconvergent paths, and (3) high-fanout nets.



Globally-Aware Dynamic Optimization. A GA generates bespoke sequences per partition. To avoid suboptimal local gains, we introduce a lightweight, globally-aware fitness function. It estimates the global Node-Depth Product (NDP) by projecting local changes, explicitly accounting for critical paths to maximize true circuit quality.

$$N_g' = N_g - \Delta N_l.$$

$$D_g' = \begin{cases} D_g - \Delta D_l, & \text{if on crit. path,} \\ \max(D_g, D_{l,\text{new}}) - \lambda \cdot \Delta D_l, & \text{otherwise.} \end{cases}$$

Evaluation

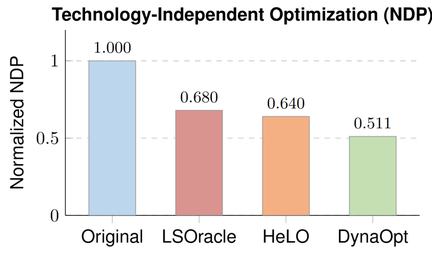
TABLE I Technology-independent logic optimization result. NDP denotes the product of node count and depth.

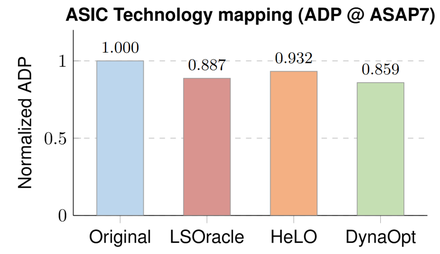
Circuit	Original			LSOracle [14]			HeLO [10] *			DynaOpt (Ours)		
	node	level	NDP	node	level	NDP	node	level	NDP	node	level	NDP
pico-rv	14551	31	451081	15124	18	272232	19268	18	346824	12780	15	**191700**
chip_bridge	58596	31	1816476	59180	19	1124420	58317	19	1108023	57532	17	**978044**
s38417	8594	28	240632	9198	19	174762	9522	16	152352	8271	16	**132336**
fpu	65750	33	2169750	60955	20	1219100	68099	20	1361980	60466	18	**1088388**
aes_core	13232	44	582208	14318	29	415222	21867	18	393606	9968	26	**259168**
des_perf	82373	20	1647460	79784	16	1276544	70176	15	**1052640**	76482	14	1070748
ethernet	67164	33	2216412	64909	22	1427998	71896	20	1437920	61065	20	**1221300**
dyn_node	3986	27	107622	4113	19	78147	4034	18	72612	3798	14	**53172**
vga_lcd	105334	22	2317348	102031	19	1938589	101534	17	1726078	103788	15	**1556820**
fpga_bridge	318081	41	13041321	312498	31	9687438	324356	24	7784544	322419	20	**6448380**
i2c	1342	20	26840	1404	10	14040	1385	8	11080	1168	8	**9344**
mem_ctrl	46836	114	5339304	52819	69	3644511	56592	61	3452112	46258	54	**2497932**
normalize	1.000	1.000	1.000	1.018	0.669	0.680	1.106	0.591	0.640	0.929	0.551	**0.511**

TABLE II ASIC technology mapping result using ASAP7 PDK. ADP denotes the product of delay (ps) and area (um^2).

Circuit	Original			LSOracle [14]			HeLO [10] *			DynaOpt (Ours)		
	area	delay	ADP	area	delay	ADP	area	delay	ADP	area	delay	ADP
pico-rv	700.7	325.2	227850.4	618.6	269.5	166728.6	831.6	290.0	241153.0	564.0	283.8	**160051.9**
chip_bridge	2657.2	308.9	820871.5	2613.4	293.6	**767247.8**	3028.2	263.9	799010.0	2512.1	317.1	796448.6
s38417	418.7	314.7	131790.0	428.9	296.7	127280.7	416.2	266.7	**111016.0**	420.6	296.2	124578.0
fpu	2751.4	396.5	1090926.1	2765.4	341.0	**943098.4**	3127.9	324.8	1016209.0	2873.2	336.0	965449.3
aes_core	573.1	511.8	293308.1	615.6	441.7	271895.5	1061.0	251.0	266276.0	562.0	451.9	**253954.4**
des_perf	4459.3	264.8	1180943.2	4492.9	239.1	1074117.6	3457.8	232.8	**804807.0**	4210.7	249.1	1049009.2
ethernet	3131.6	345.1	1080736.1	2872.1	342.4	983464.5	3407.0	289.4	985948.0	2739.1	314.5	**861461.8**
dyn_node	190.1	299.5	56932.0	196.5	241.0	**47353.2**	205.5	231.7	47610.0	199.4	240.9	48026.2
vga_lcd	4766.1	387.1	1844898.0	4676.2	340.2	1591043.9	5627.5	259.5	1460459.2	4292.4	338.8	**1454100.2**
fpga_bridge	14044.7	515.1	7234430.1	14997.7	430.1	6451123.6	16385.7	340.9	**5585048.8**	14458.8	455.7	6588735.1
i2c	53.2	132.1	7024.8	60.3	107.0	6451.3	60.2	131.7	7931.6	57.4	107.4	**6164.6**
mem_ctrl	1826.5	997.9	1822553.1	1935.5	849.0	1643125.7	2395.2	1021.3	2446214.2	1841.7	826.8	**1522807.8**
normalize	1.000	1.000	1.000	1.014	0.877	0.887	1.170	0.812	0.932	0.972	0.886	**0.859**

HeLO* is non-open source, and results are quoted from original paper. The discrepancy primarily arises from Verilog-to-AIG conversion.





Ablation Study (Normalized NDP)

Full DynaOpt	**0.266**
w/o Aware-Part	0.282
w/o Pre-Opt	0.322
w/o Dynamic-Seq	0.377

DynaOpt significantly outperforms LSOracle and the SOTA HeLO. It reduces average normalized NDP to 0.511 (best on 11/12 benchmarks), achieving a 24.9% improvement over baselines. Post-mapping to ASAP 7nm confirms these logic-level gains, delivering the lowest ADP of 0.859. Finally, ablation studies confirm dynamic sequence discovery is the primary performance driver.

Conclusion

DynaOpt is an adaptive heterogeneous logic optimization framework. It combines timing/structure-aware partitioning, GNN-based DAG selection, and a Genetic Algorithm guided by a globally-aware fitness metric to generate custom optimization sequences per sub-circuit. DynaOpt significantly outperforms SOTA baselines, establishing a highly adaptive new paradigm for logic synthesis.

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